1.1.1 Structure and function of the processor – DIL notes

Specification sections covered in this week's exercises:

Name:

Section number	Sub section	Description
Playlist: https://www.youtube.com/playlist?list=PLCiOXwirraUB7V2i0SJ4SSJFqRV_LtgzW		
1.1.1 Structure and function of the processor	1.1.1 (a)	The Arithmetic and Logic Unit; ALU, Control Unit and Registers (Program Counter; PC, Accumulator; ACC, Memory Address Register; MAR, Memory Data Register; MDR, Current Instruction Register; CIR). Buses: data, address and control: how this relates to assembly language programs.
	1.1.1 (b)	The Fetch-Decode-Execute Cycle; including its effects on registers.
	1.1.1 (c)	The factors affecting the performance of the CPU: clock speed, number of cores, cache.
	1.1.1 (d)	The use of pipelining in a processor to improve efficiency.
	1.1.1 (e)	Von Neumann, Harvard and contemporary processor architecture.

Key terms

Explain the following below:

CPU, ACC, PC, Control unit, CIR, MDR, Control bus, Data bus, Address bus, ALU, Register, Buses, Assembly language, Fetch-decode-execute, Cores, Cache, Clock speed, Pipelining, Von Neumann architecture, Harvard architecture, Contemporary architecture.

CPU

ACC

PC

Control unit

CIR

MDR

Control bus

Data bus

Address bus

ALU, Register

Buses

Assembly language

Fetch-decode-execute

Cores

Cache

Clock speed

Pipelining

Von Neumann architecture

Harvard architecture

Contemporary architecture

Topic: 1.1.1(a) The Arithmetic and Logic Unit; ALU, Control Unit and Registers (Program Counter; PC, Accumulator; ACC, Memory Address Register; MAR, Memory Data Register; MDR, Current Instruction Register; CIR). Buses: data, address and control: how this relates to assembly language programs.
https://youtu.be/UdHK35N-Kuo

Questions:	Notes:

Summary:

Topic: 1.1.1(b) The Fetch-Decode-Execute Cycle; including its effects on registers.
https://youtu.be/OTDTdTYId2g

Questions:	Notes:

Summary:

Topic: 1.1.1 (c) The factors affecting the performance of the CPU: clock speed, number of cores, cache.
https://youtu.be/Nz2JJXYKWJc

Questions:	Notes:

Summary:

Topic: 1.1.1 (d) The use of pipelining in a processor to improve efficiency.
https://youtu.be/ULUb4xwqz4A

Questions:	Notes:

Summary:

Topic: 1.1.1 (e) Von Neumann, Harvard and contemporary processor architecture.
https://youtu.be/4WFzOyUNkaM

Questions:	Notes:

Summary: